Amendments to the Specification

Please replace paragraph 45, beginning on page 9, line 5, with the following rewritten paragraph:

[45]   The parallel CRC encoder uses register stages 460-466 that are connected together by exclusive-or gates 470-478 as shown in Figure 4C. The parallel CRC encoder becomes somewhat more complicated, however, with the simple exclusive-or gates (360-368) in the serial case replaced by a more complex exclusive-or logic tree 480 as indicated in Figure 4C. Logic tree 480 generates the same function of its contents that would be obtained by shifting the register in Figure 3C n times, with n the length of the register. For example, let $n = 4$ and let the contents of the last stage be fed back into the first and second stages (so that $g(x) = x^4 + x + 1$). Then, as is easily verified, the contents of the first through the fourth stages of the shift-register after four shifts are $x_0 + x_3$, $x_0 + x_2 + x_3$, $x_1 + x_2$, $x_0 + x_1$, respectively, with x_0, x_1, x_2 and x_3 the initial contents of those stages, and the exclusive-OR logic is defined accordingly. (The symbol "+" here indicates addition over the binary field, i.e., the exclusive-OR operation.)

Please replace paragraph 52, beginning on page 11, line 3, with the following rewritten paragraph:

[52]   Since the ingress and egress headers are generally different, the egress information consists of the ~~catenation~~ concatenation of the egress header 516 with the data portion of the ingress information as indicated schematically by arrow 514. The multiplexer 506 is used to concatenate the new header 516 with the ingress data 514 to produce the egress information 518.